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alloys, and other alloys of these metals; lossy ferrite materials such as Ni
ferrite or Mn ferrite, or magnetic oxides; or
dielectric materials such as
barium titanate, strontium titanate, niobate materials, zirconate materials, or
magnetic oxides, among others, which are lossy at the frequencies of the EMI.

DEPR:
Efficiency of shielding is a strong function of the electrical and magnetic
properties of the materials used in the shield and the characteristics of the
impinging field. Electromagnetic fields can be described by the wave impedance
(Z.sub.w) which is the ratio of the magnitudes of the E- and H-field components
(Z.sub.w =E/H). Field sources which conduct relatively high currents at low
voltages are low impedance sources. Such sources may be power supply loops,
transformers, and electric motors. Fields radiated from such sources have low
Z.sub.w values, hence the ratio of E-field to H-field intensity is low.
Integrated circuits (ICs) operate at relatively high voltages compared to the
currents driven, and as such are considered high impedance signal sources.
Such signals have high Z.sub.w values due to a high E-/H-field intensity ratio.
At large distances, the Z.sub.w value from either a low or high impedance

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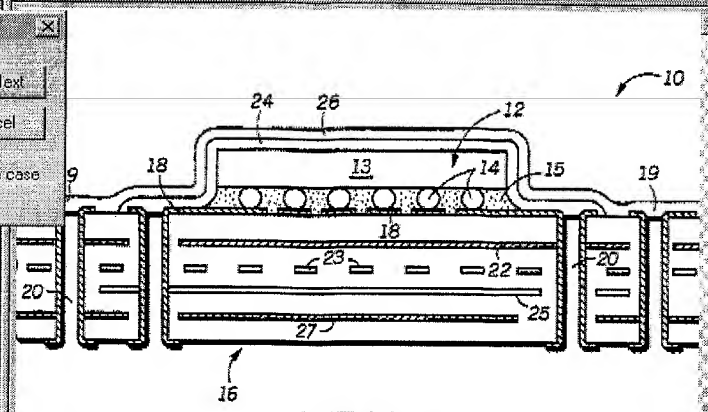
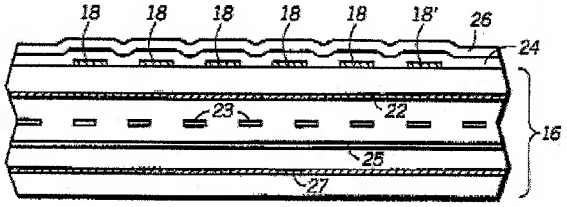


FIG.1



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US006097080A

United States Patent [19]

Nakanishi et al.

[11] Patent Number: 6,097,080

[45] Date of Patent: Aug. 1, 2000

[54] **SEMICONDUCTOR DEVICE HAVING MAGNETIC SHIELD LAYER CIRCUMSCRIBING THE DEVICE**

[75] Inventors: **Tsutomu Nakanishi**, Tokyo; **Akira Okamoto**, Saitama, both of Japan

[73] Assignees: **Susumu Okamura**; **Takeshi Ikeda**, both of Tokyo, Japan

[21] Appl. No.: **09/171,455**

[22] PCT Filed: **Apr. 23, 1997**

[86] PCT No.: **PCT/JP97/01412**

§ 371 Date: **Oct. 19, 1998**

§ 102(e) Date: **Oct. 19, 1998**

[87] PCT Pub. No.: **WO97/40654**

PCT Pub. Date: **Oct. 30, 1997**

[30] **Foreign Application Priority Data**

Apr. 24, 1996 [JP] Japan 8-127783

[51] **Int. Cl.**[7] **H05K 1/00**

[52] **U.S. Cl.** **257/659**; 257/660; 257/661; 257/676; 257/687; 257/700

[58] **Field of Search** 257/659, 660, 257/661, 676, 687, 700

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,151,770 9/1992 Inoue .
5,151,771 9/1992 Hiroi et al. 257/676
5,286,926 2/1994 Kimura et al. .

FOREIGN PATENT DOCUMENTS

0 408 228 1/1991 European Pat. Off. .
0 503 200 9/1992 European Pat. Off. .
59-162762 10/1984 Japan .
1-78037 5/1989 Japan .
3-214691 9/1991 Japan .
5-79995 10/1993 Japan .

OTHER PUBLICATIONS

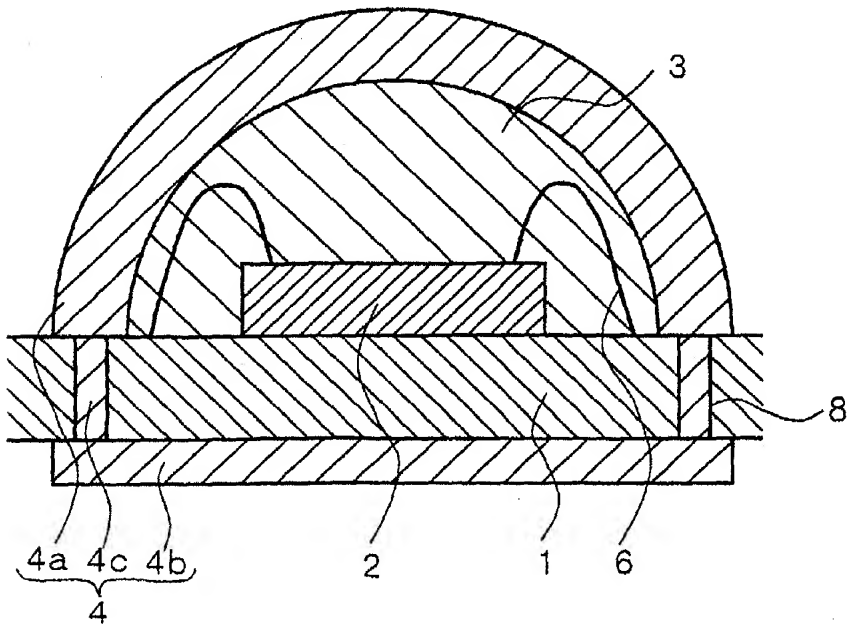
Patent Abstracts of Japan, vol. 017, No. 504 (E–1430) Sep. 10, 1993, JP–A–05 129 793 (Abstact) May 25, 1993.

Primary Examiner—Fetsum Abraham
Attorney, Agent, or Firm—Dellett and Walters

[57] **ABSTRACT**

It is the object to minimize a magnetic influence, on the outside, of a semiconductor chip which is formed on a substrate includes inductor conductors. A semiconductor chip **2** including inductor conductors is mounted on a substrate **1** and a plurality of through holes **8** are formed in the area on the outside of the mounting position. Shielding members **4** are formed on the chip mounting side and the opposite side of the substrate **1** and in the through holes **8** so as to cover the semiconductor chip **2** with the shielding members **4** from both sides of the substrate **1**. Therefore, magnetic fluxes from a circuit formed on the semiconductor chip **2** do not leak out from the shielding members **4**, but circulate inside the shielding members **4**.

6 Claims, 3 Drawing Sheets



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BSPR:
The first type includes those substrates which are made primarily of resins,
such as a resin plate and a laminated plate obtained by laminated-molding of
prepregs which are prepared by drying after impregnating the base material with
varnish of the thermosetting resin. The substrates of the first type are most
widely used because they have the principal characteristics required for the
substratres for wiring boards, such as having superior electric isulation. On
the other hand, the high density of the contemporary semiconductor chips
generates substantial heat therein and as a result, an escape for such heat has
become a great concern. In addition, the noise level becomes annoying unless a
magnetic shield is provided. In these regards, it has been recognized that
those first type substrates suffer from a lack of heat releasing capability and
magnetic shield effect as well.

BSPR:
The second type includes those made of a metal plate as a core extending in the
middle of the board and being referred to as a metal core board. The specific
structure and performance of the metal core boards are extensively diclosed,
for example, in IPC Standard 1985 by The Institute for Interconnecting and
Packaging Electronic Circuits and the Hewlett-Packard Journal (August 1983).
The substrates of the second type display a superior property regarding the
heat releasing capability and the magnetic shield effect. However, they have
an inherent disadvantage in securing electric insulation particularly between
the leads and the metal core which are located very close to each other. This
is particularly true with the LCC (Leadless Chip

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United States Patent [19]
Higuchi et al.

[11] Patent Number: 4,835,598
[45] Date of Patent: May 30, 1989

[54] WIRING BOARD

[75] Inventors: Yasuo Higuchi; Toshiyuki Yamaguchi; Takashi Kasuo, all of Kadoma, Japan

[73] Assignee: Matsushita Electric Works, Ltd., Osaka, Japan

[21] Appl. No.: 52,182

[22] Filed: May 14, 1987

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 784,597, Nov. 8, 1985, abandoned.

[30] Foreign Application Priority Data

Jun. 15, 1984 [JP] Japan 59-123517
Jul. 13, 1984 [JP] Japan 59-154755

[51] Int. Cl.[4] H01L 23/34; H01L 23/14; H01L 23/40

[52] U.S. Cl. 357/79; 357/80; 357/81

[58] Field of Search ..... 357/80, 72, 81, 79; 174/52 FP, 16 HS

[56] References Cited

U.S. PATENT DOCUMENTS

3,853,658 5/1974 Burns 357/72
3,916,488 2/1975 Queenan et al. 357/80
4,150,389 4/1979 Wilson et al. 357/80
4,218,701 8/1980 Hilbrandt 357/72
4,322,616 3/1982 Bickel et al. 357/80
4,574,387 3/1985 Sachi 357/80

4,596,836 5/1983 Mallory et al. 357/80
4,638,098 4/1986 Baldwin et al. 357/81
4,646,709 10/1986 Nakaya et al. 357/81
4,656,502 10/1987 Young et al. 357/81

FOREIGN PATENT DOCUMENTS

0058455 5/1980 Japan 357/74
0109065 7/1982 Japan 357/81

OTHER PUBLICATIONS

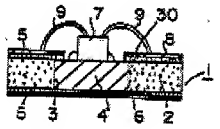
"Microcircuit Heat Sink"-Chernack et al.-IBM Technical Disclosure Bulletin-vol. 8, No. 10, Mar. 1966, p. 1457.

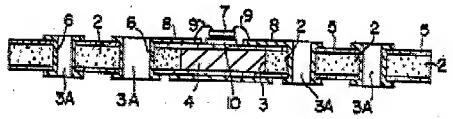
Primary Examiner—Andrew J. James
Assistant Examiner—S. V. Clark
Attorney, Agent, or Firm—Koda and Androlia

[57] ABSTRACT

A printed wiring board for carrying a semiconductor chip including a resin base substrate having at least one opening therethrough, a thermo-conductive plate for mounting the semiconductor chip thereon, the plate being inserted into the opening, an insulating adhesive layer covering at least one side of the substrate and an electric circuit formed on the layer. The wiring board of this invention eliminates those disadvantages of the existing resin substrate type and metal core type. In essence, the wiring board of this invention displays excellent heat releasing capability and magnetic shield effect as well as reliable electric insulation.

8 Claims, 4 Drawing Sheets





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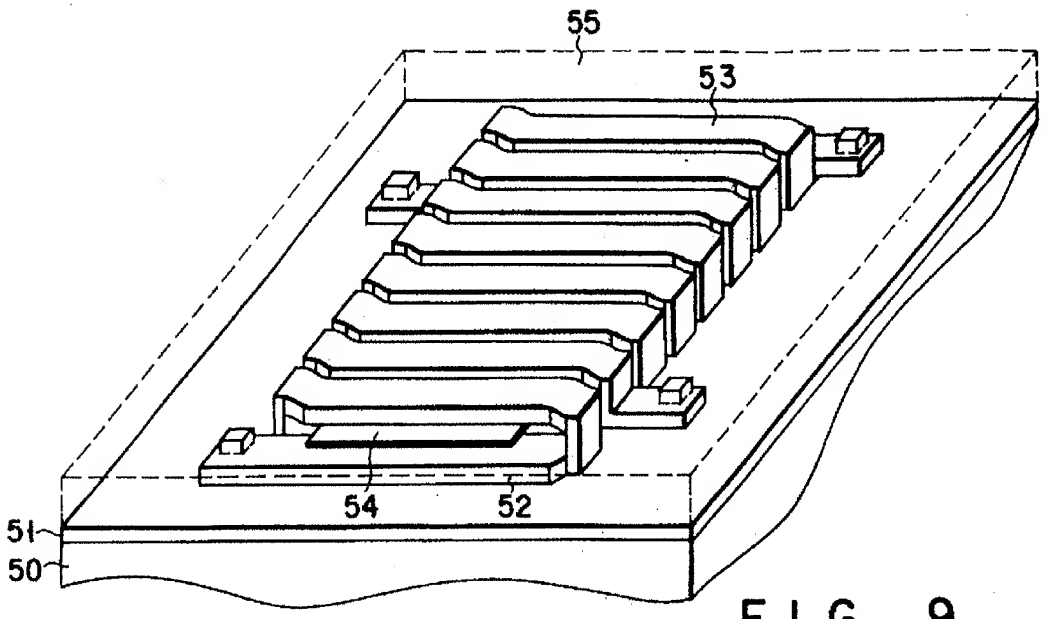


FIG. 9

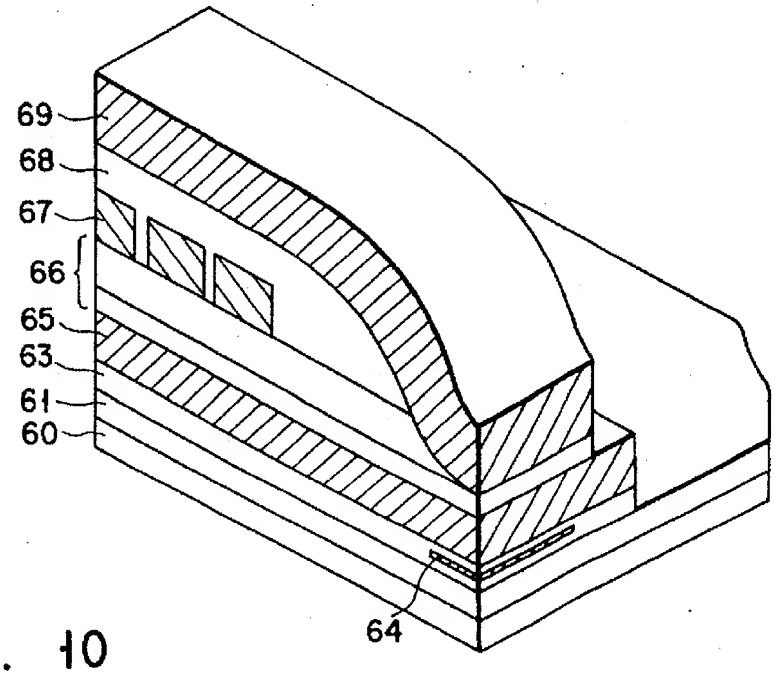


FIG. 10

US005851681A

United States Patent [19]

Matsuyama et al.

[11] Patent Number: 5,851,681

[45] Date of Patent: Dec. 22, 1998

[54] **WIRING STRUCTURE WITH METAL WIRING LAYERS AND POLYIMIDE LAYERS, AND FABRICATION PROCESS OF MULTILAYER WIRING BOARD**

[75] Inventors: **Haruhiko Matsuyama**, Hiratsuka; **Eiji Matsuzaki**, Yokohama; **Shozi Ikeda**, Yokohama; **Fumio Kataoka**, Yokohama; **Fusaji Shoji**, Yokohama, all of Japan

[73] Assignee: **Hitachi, Ltd.**, Tokyo, Japan

[21] Appl. No.: **212,766**

[22] Filed: **Mar. 15, 1994**

[30] **Foreign Application Priority Data**

Mar. 15, 1993 [JP] Japan 5-054318

[51] **Int. Cl.**[6] **G11B 5/40**; C08G 69/26

[52] **U.S. Cl.** ..... **428/473.5**; 428/209; 428/458; 428/694 ML; 174/258; 528/353

[58] **Field of Search** ..... 428/209, 473.5, 428/615, 618, 458, 694 ML; 174/258

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,587,197	5/1986	Kojima et al.	430/196
4,686,147	8/1987	Matsuyama et al.	428/447
4,772,505	9/1988	Matsuyama et al.	428/209
4,824,731	4/1989	Matsuyama et al.	428/473.5
5,208,656	5/1993	Matsuyama et al.	174/253
5,601,905	2/1997	Watanabe et al.	428/215

FOREIGN PATENT DOCUMENTS

63-143846 6/1988 Japan .

OTHER PUBLICATIONS

Shih, et al., 42nd Electric Compounds and Technology Conference, pp. 1002–1014, 1992.

U.S. Ser. No. 7742044, filed Aug. 8, 1991.

Advanced Organic Chemistry, 3rd Edition; Francis A. Carey and Richard J. Sundberg.

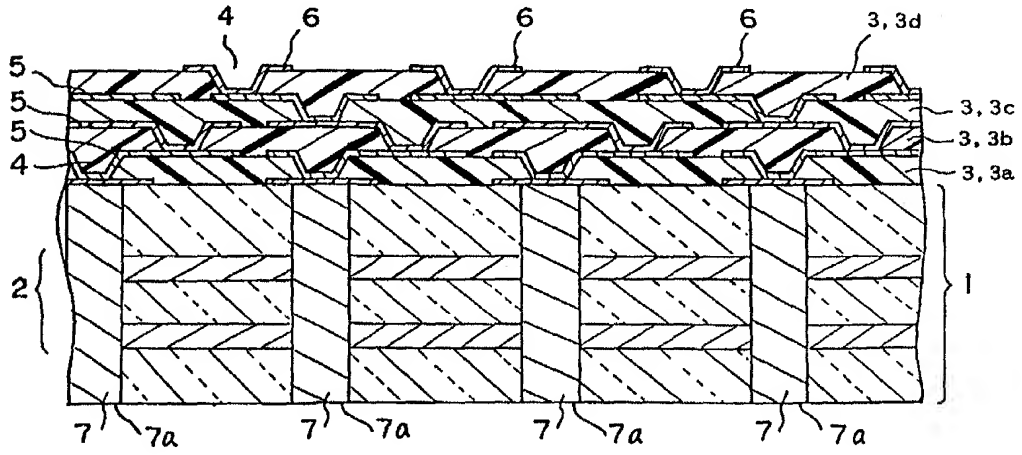
Primary Examiner—Cathy F. Lam

Attorney, Agent, or Firm—Antonelli, Terry, Stout & Kraus, LLP

[57] **ABSTRACT**

This invention relates to a wiring structure having metal wiring layers and polyimide layers. An object of this invention is to overcome problems caused by oxidation of a metal surface, such as an increase in the resistance of wiring and a reduction in insulation, by preventing a reaction between a metal of the wiring layers, such as copper, and carboxyl groups of polyamic acid which make up the polyimide layers. In the wiring structure according to the present invention, the polyimide layers have been formed by heating and curing a resin composition which comprises a polyimide precursor, an amine compound and an organic solvent.

14 Claims, 1 Drawing Sheet



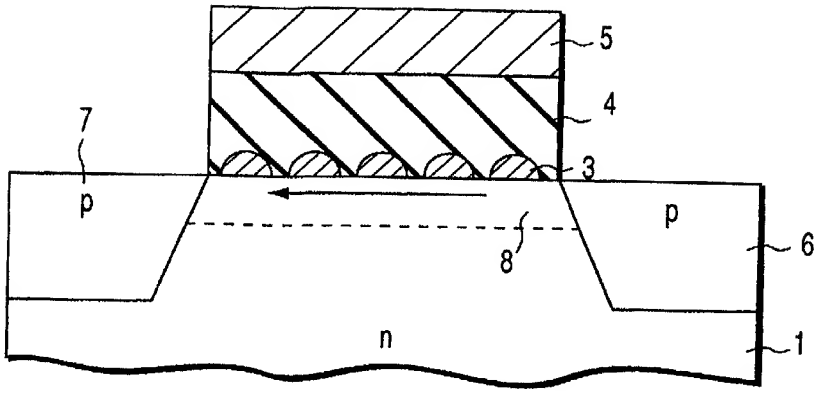


FIG. 5

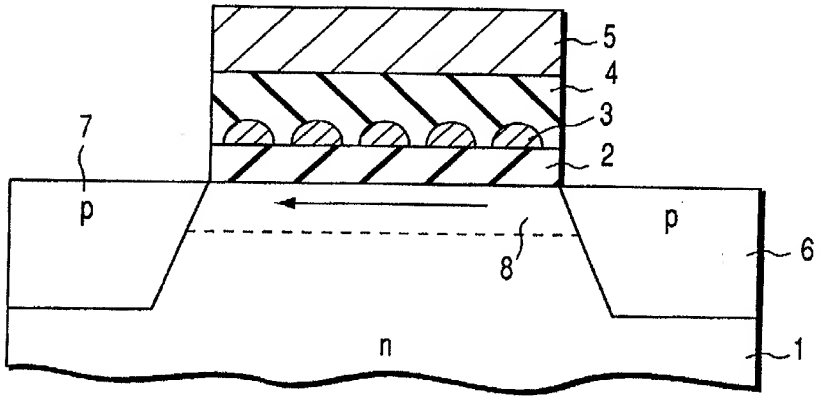


FIG. 6

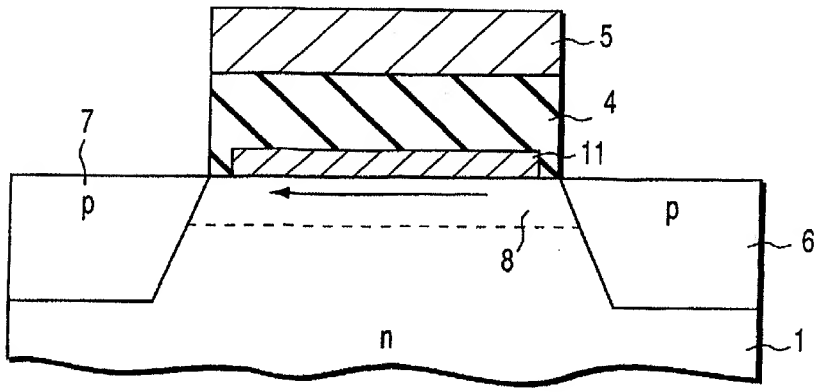


FIG. 7A

FIG. 3

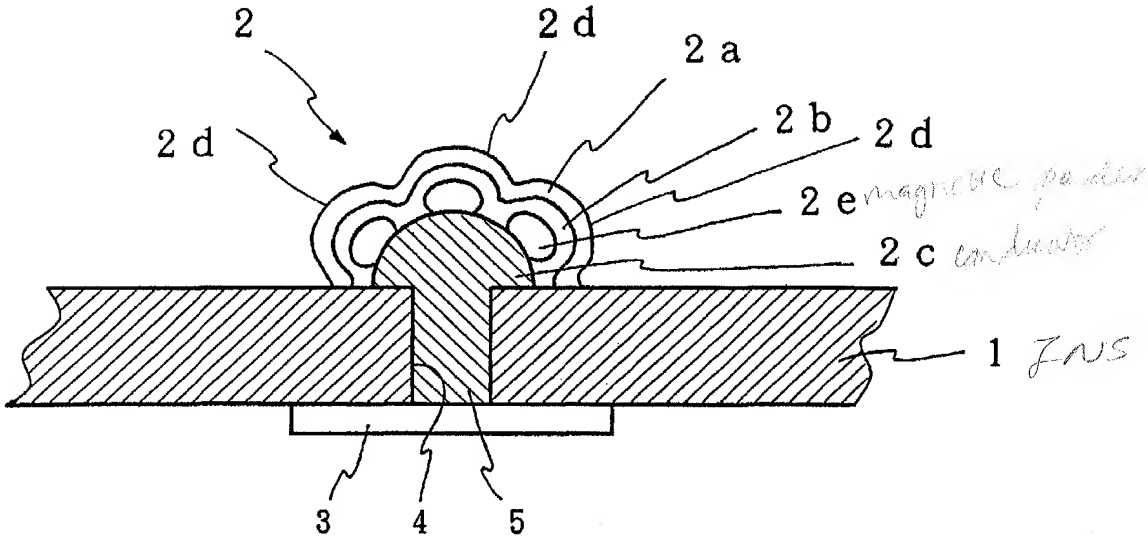
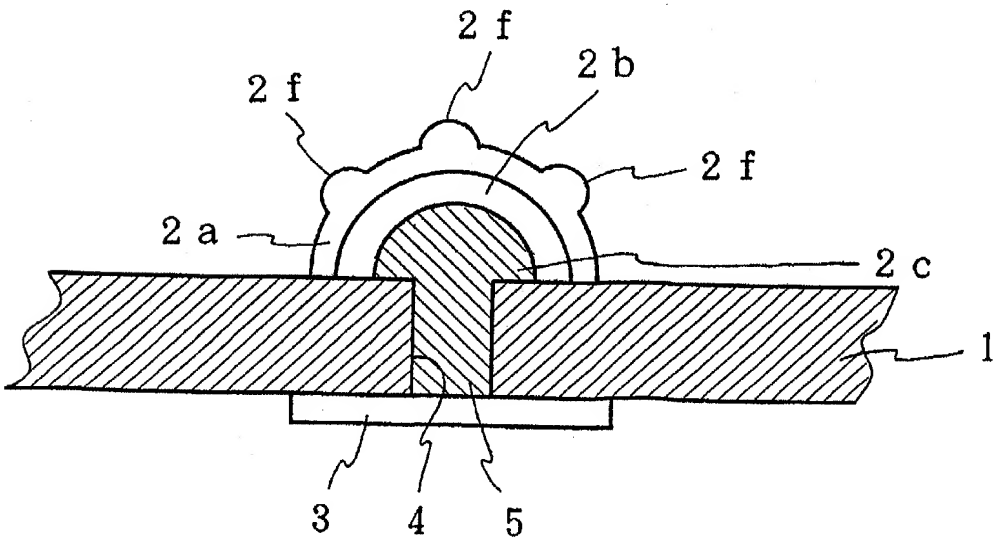


FIG. 4



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strip conductor 9 is formed on the lower surface of the dielectric layer 2B,
the first MS line 8 is constituted by the interaction of the strip conductor 7
and the ground layer 6, and the second MS line 10 is constituted by the
interaction of the strip conductor 9 and the ground layer 6.

DEPR:
An increase in the current just on the slot 11 results in an increase in the
intensity of the magnetic field at this place, and a magnetic field is
generated accompanied by an intense magnetic field encircling the strip
conductor 7 of the MS line 8. Upon adjusting the length SL of the slot 11,
therefore, an intense electromagnetic field is excited in the slot 11 due to
the magnetic field generated by the MS line 8. Then, an electromagnetic field
is generated even by the MS line 10 of the lower surface accompanied by an
intense magnetic field which encircles the strip conductor 9, and
high-frequency signals fed to the MS lines 8 are transmitted to the MS line 10
through the slot 11.

DEPR:
The magnetic field of high-frequency signals transmitted over the transmission
line assumes an encircling form on a plane perpendicular to the MS line at all
times unlike that of the case of when a via hole conductor is used, and
migrates from the MS line 8 to the MS line 10 through the slot 11 in an

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FIG. 1

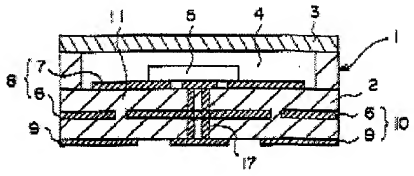
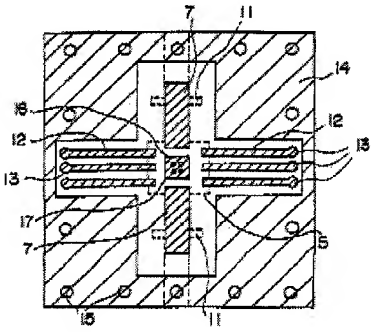


FIG. 2



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